UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/679,928	10/06/2003	Louise A. Koss	10011462-2	2922

7590 04/12/2004

AGILENT TECHNOLOGIES, INC.
Legal Department, DL429
Intellectual Property Administration
P.O. Box 7599
Loveland, CO 80537-0599

EXAMINER	
PHAM, LY D	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 04/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/679,928	KOSS ET AL.	
	Examiner	Art Unit	
	Ly D Pham	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 6-9* is/are rejected.

7)☒ Claim(s) *3-5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 9 are presented for the examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, and 6 – 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lattimore et al. (US Pat 6,185,709 B1) in view of Kablanian et al. (US Pat 5,764,878).

Regarding **claims 1 and 7**, Lattimore et al. disclose an electronic circuit for self-repair of a random access memory array, comprising:

a write selector circuit with each slice array (fig. 2, I/O circuit 208 for write/read operations), wherein the random access memory is organized into a plurality of slice arrays (abstract: "...the memory to which the redundant sub-array is added is typically an on-chip memory which is organized into bit-slice sub-arrays."), wherein each slice array comprises at least one memory storage cell, and wherein at least one of the slice arrays is redundant (abstract: redundant sub-arrays);

a read selector circuit associated with each slice array(fig. 2, I/O circuit 208);

a remap register associated with each slice array (col. 7, lines 42 – 50, or col. 8, lines 33 – 45, "... redundancy control circuit 304 may be implemented as a register ..."), wherein when power is applied to the circuit, the circuit automatically performs a self-test (col. 7, lines 40 – 42) and wherein when the self-test detects a defect, the remap register of the slice array having the defect is set to indicate the presence of the defect resulting in the associated remap selector circuit instructing the associated write selector circuit to redirect data intended for storage in that slice array to an adjacent slice array and instructing the associated read selector circuit to redirect data read from the adjacent slice array to the output of the defective slice array (col. 9, line 54 – col. 10, line 19: "...each of the data values which are accessed corresponding to the requested address are shifted to the right and provided to a **next sub-array.** Therefore, data value DI2 is provided to sub-array 3 422 via multiplexer 414 and data value DIn is provided to **sub-array n+1** 424.")

Though Lattimore et al. did not call the redundancy control register as a remap register, method of such application has been shown by Kablanian et al. (fig. 1 and col. 4, lines 3 – 23: "Remapper 16 redirects original address locations of defective memory access the address locations which can retain valid data." This means that if the adjacent addressed storage location is non-defective, it can certainly used to replace the one next to it. Also, col. 7 , lines 4 – 17 further show I/O remapping circuit 150 included in remapper circuit 16 and to be controlled by FLARE circuit. I/O remapping circuit 150 operates as remap selector circuit which instruct operations of associated read/write selector circuit, which is I/O circuit).

Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to combine the disclosures of Lattimore et al. and Kablanian et al. so that the memory circuit includes BISR and BIST capabilities (Kablanian et al., col. 2, line 44 – col. 3, line 40).

Regarding **claim 2**, the electronic circuit as recited in claim 1, wherein when a slice array is tested to be defect free, the remap register then set the associated remap selector circuit to permit data read/write to that slice array. It is considered common and well known in the art where redundancy applications and methods are provided for curing problems with cells defects and there is no reason why replacement is necessary as the memory array is found defect free. An examplified remapping circuit such as Kablanian's discloses that data are redirected/remapped to non-defect location ONLY when a defect to where data are intended for storage is found. Therefore, feature as claimed in claim 2 is considered inherent to Kablanian's disclosure.

Regarding **claims 6, 8, and 9**, Lattimore et al. also show the electronic circuit as recited in claim 1, wherein the electronic circuit is embedded within a bit-slice in an IC, wherein the bit-slice comprises the slice array and other circuitry associated with the slice array (col. 1, lines 5 – 36 and col. 9, lines 54 – 58).

4. Claims 6, 8, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lattimore et al. (US Pat 6,185,709 B1) and Kablanian et al. (US Pat 5,764,878), further in view of Dreibelbis et al. (US Pat 6,185,709).

Regarding **claims 6, 8, and 9**, the electronic circuit as recited in claim 1, wherein the electronic circuit is embedded within a bit-slice in an IC, wherein the bit-slice comprises the slice array and other circuit associated with the slice array. This feature has also been shown by Dreibelbis et al. (abstract, col. 3, lines 47 – 49). Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to incorporate the feature shown by Dreibelbis et al. to the disclosures by Lattimore et al. and Kablanian et al. to provide a device for testing the fixability a logic circuit using specific testing pattern (col. 2, lines 14 – 55).

Allowable Subject Matter

5. **Claims 3 – 5** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior arts show an electronic circuit for self-repair of a RAM array as claimed in claims 1, 2, and 6 – 9. However, the prior arts fail to further show:

The remap selector circuit associated with each slice array comprises an OR gate, wherein the OR gate has a 2 inputs and one output. The first input is connected to the OR-gate output associated with the adjacent higher-numbered slice array, wherein the second input is connected to the output of the remap register, and wherein the output is connected to the input of the write and read selector circuits.

And

The write selector circuit associated with each slice array comprises a write multiplexer, wherein the write multiplexer has afirst write-multiplexerinput, a second write-multiplexer input, a write-multiplexer control input, and a write-multiplexer output, wherein the write-multiplexer control input is connected to the output of the remap selector circuit, wherein the first write-multiplexer input is connected to the second write-multiplexer input associated with the adjacent higher-numbered slice array, wherein the second write-multiplexer input is connected to an output of an input register, and wherein the write-multiplexer output is capable of transfening data to the slice array.

And

The read selector circuit associated with each slice array comprises a read multiplexer, wherein the read multiplexer has a first read-multiplexer input, a second read-multiplexer input, a read-multiplexer control input, and a read-multiplexer output, wherein the read-multiplexer control input is connected to the output of the remap selector circuit, wherein the first read-multiplexer input is capable of obtaining data from the slice array, wherein the second read-multiplexer input is connected to the first read-multiplexer input associated with the adjacent lowered-numbered slice array, and wherein the read-multiplexer output is capable of transferring data to an output register.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. When responding to the office action, Applicant(s) are advised to provide the examiner with the page and line numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

8. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

9. Any inquiry concerning this communication on earlier communications from the examiner should be directed to Ly Pham, whose telephone number is **571-272-1793**. The examiner can normally be reached on Monday – Friday from 8:30am to 5:00pm, alternate Friday off. The examiner's supervisor, David Nelms, can be reached at **571-272-1787**. The fax number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Ly Pham

April 6, 2004

David Nelms
Supervisory Patent Examiner
Technology Center 2800